

Figure 1

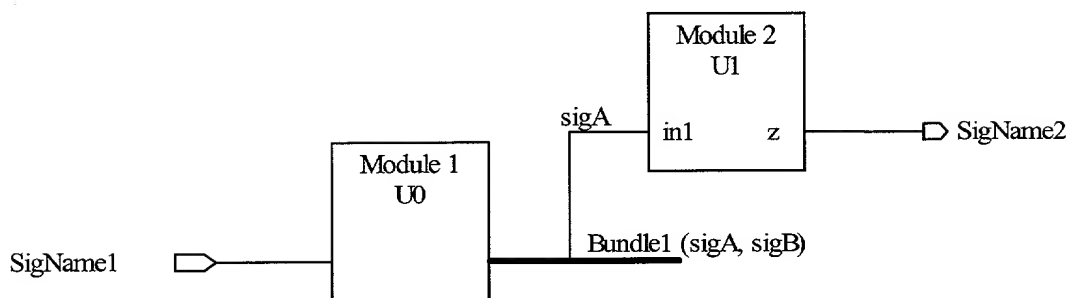


Figure 2

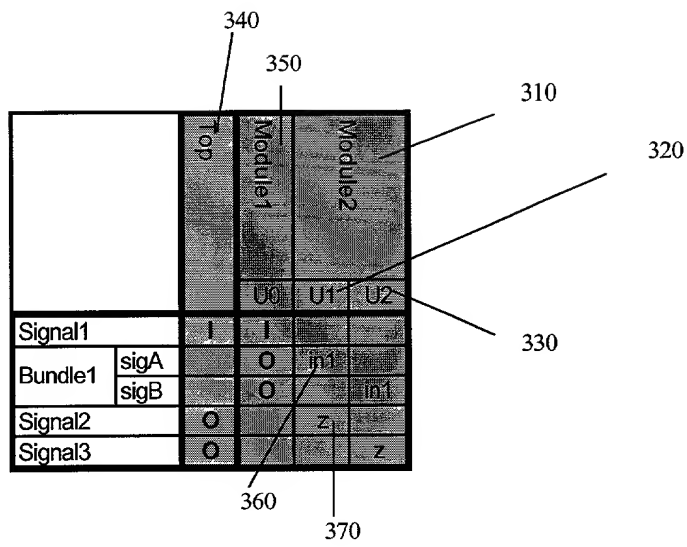


Figure 3

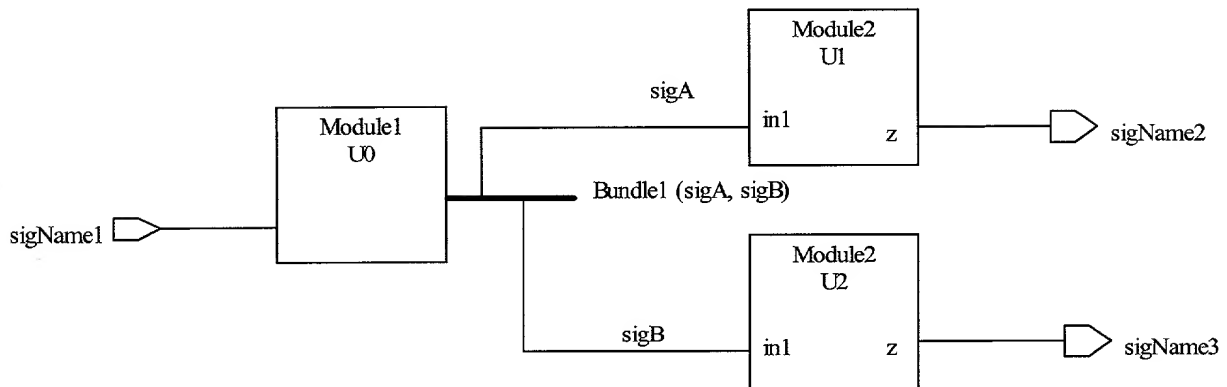


Figure 4

```

503 LIBRARY ieee;
504 USE ieee.std_logic.all;
505
506 ENTITY Top IS
507     port (Signal1 : IN std_logic;
508           Signal2 : OUT std_logic
509           Signal3 : OUT std_logic);
510 END Top;
511
512 ARCHITECTURE struct OF Top IS
513
514     SIGNAL sigA      : std_logic;
515     SIGNAL sigB      : std_logic;
516
517     COMPONENT Module1
518     PORT(
519         Signal1      : IN std_logic;
520         sigA          :OUT std_logic;
521         sigB          :OUT std_logic;
522     );
523     END COMPONENT;
524
525     COMPONENT Module2
526     PORT(
527         in1          : IN  std_logic;
528         z             : OUT std_logic;
529     );
530     END COMPONENT;
531
532 BEGIN
533
534     U0 : Module1
535         PORT MAP(
536             sigA      => sigA,
537             sigB      => sigB,
538             Signal1   => Signal1
539         );
540
541     U1 : Module2
542         PORT MAP(
543             in1 => sigA,
544             z  => Signal2
545         );
546

```

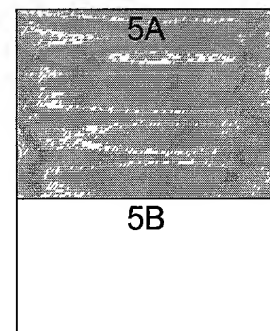


Figure 5

Figure 5A

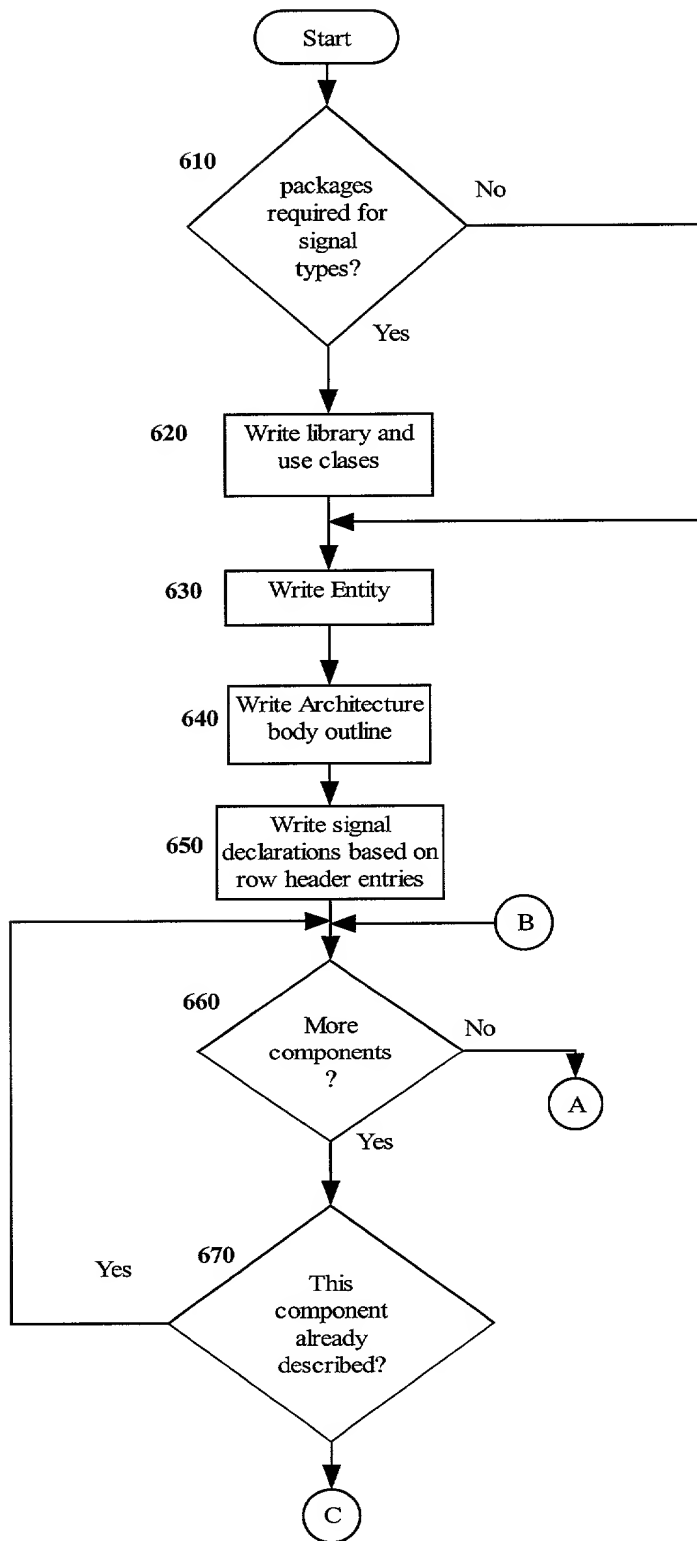


Figure 6A

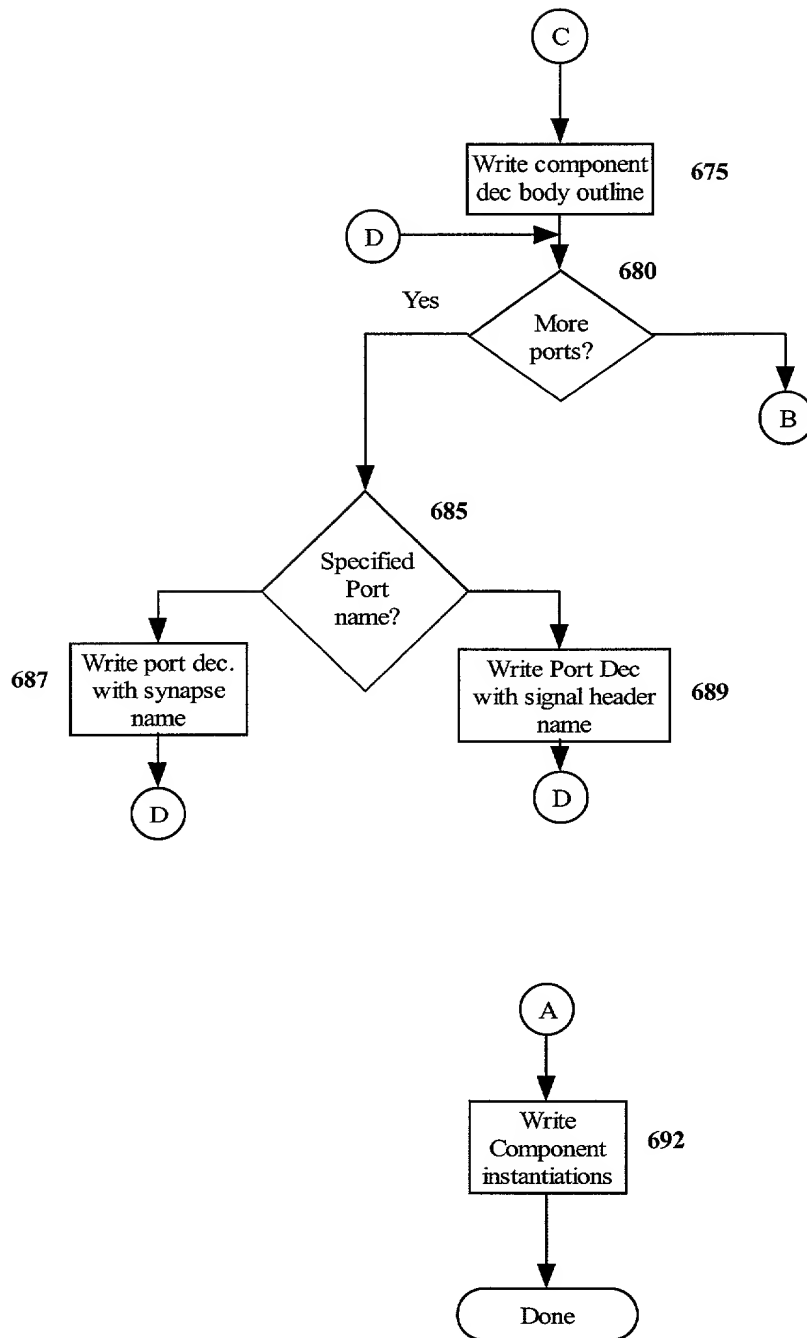


Figure 6B

	state_machine	F {A:B}	controller
inSig1	1		1
inSig2	1		1
run[6:5]	0	win[6:5]	
config[1:0]	0	end[1:0]	
outSig{A:B}		z	0

Figure 7A

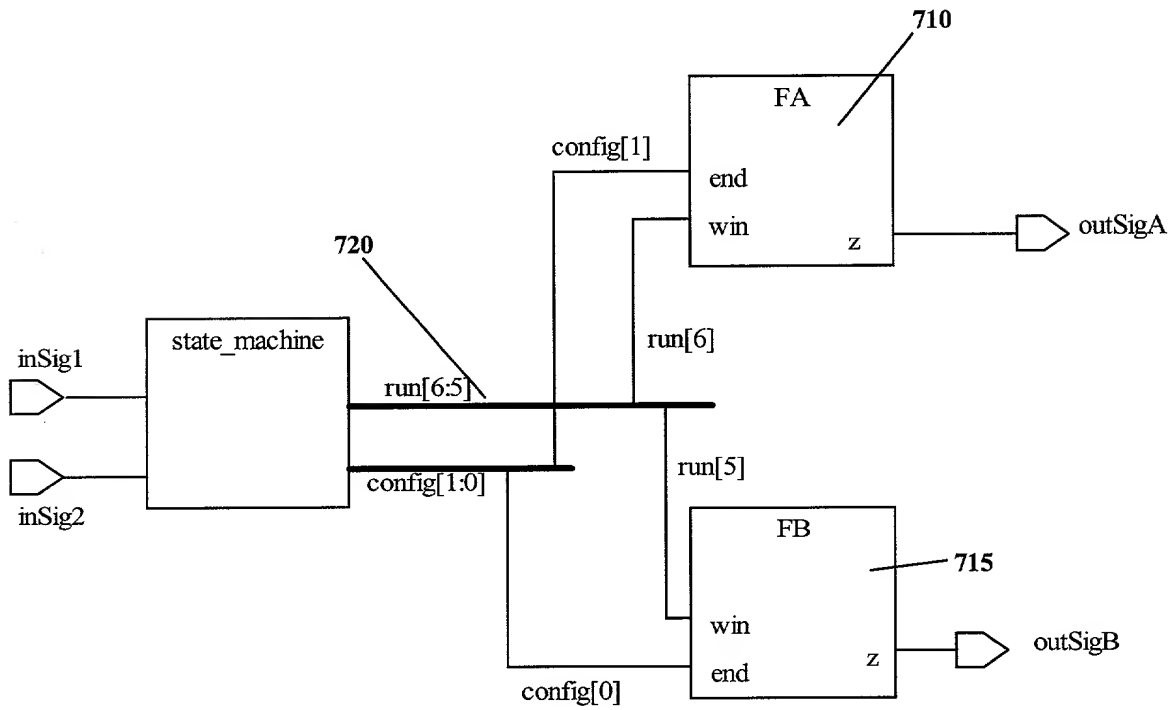


Figure 7B

Comment	Delay	Module2	Module1	Top	
Input port for top	20 ns		I	I	in1
	10 ns	I	O		intSig1
	5 ns	I	O		intSig2
Output port for top	5 ns	O		O	out1
			Rev3		cellName

Figure 8

Downloaded from www.stuvia.com

LIBRARY ieee;
USE ieee.std_logic.all;

ENTITY Top IS

PORT (in1 : IN std_logic; -- Input port for top
out1 : OUT std_logic); -- Output port for top
ATTRIBUTE delay OF IN1 : SIGNAL IS 20 ns;
ATTRIBUTE delay OF OUT1 : SIGNAL IS 5 ns;

910
920
930
940

END Top;

ARCHITECTURE struct OF Top IS

SIGNAL intSig1 : std_logic;
SIGNAL intSig2 : std_logic;
ATTRIBUTE delay OF intSig1 : SIGNAL IS 10 ns;
ATTRIBUTE delay OF intSig2 : SIGNAL IS 5 ns;

950
960

COMPONENT Module1

PORT(
in1 : IN std_logic;
intSig1 : OUT std_logic;
intSig2 : OUT std_logic;
);
END COMPONENT;

ATTRIBUTE cellName of U0 : LABEL IS "Rev3";

970

COMPONENT Module2

PORT(
intSig1 : IN std_logic;
intSig2 : IN std_logic;
out1 : OUT std_logic;
);
END COMPONENT;

BEGIN

U0 : Module1
PORT MAP(
in1 => in1,
intSig1 => intSig1,
intSig2 => intSig2
);

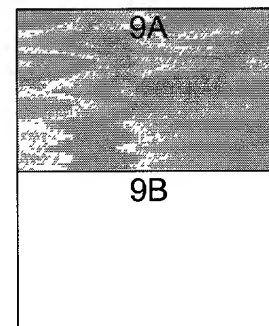


Figure 9

Figure 9A

```
U1 : Module2
  PORT MAP(
    out1  => out1,
    intSig1  => intSig1,
    intSig2  => intSig2
  );
```

```
END ARCHITECTURE struct;
```

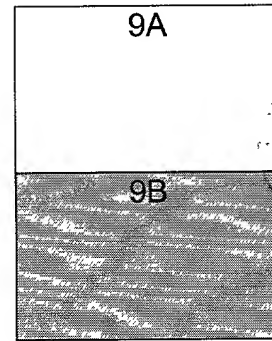


Figure 9

Figure 9B

Figure 9B

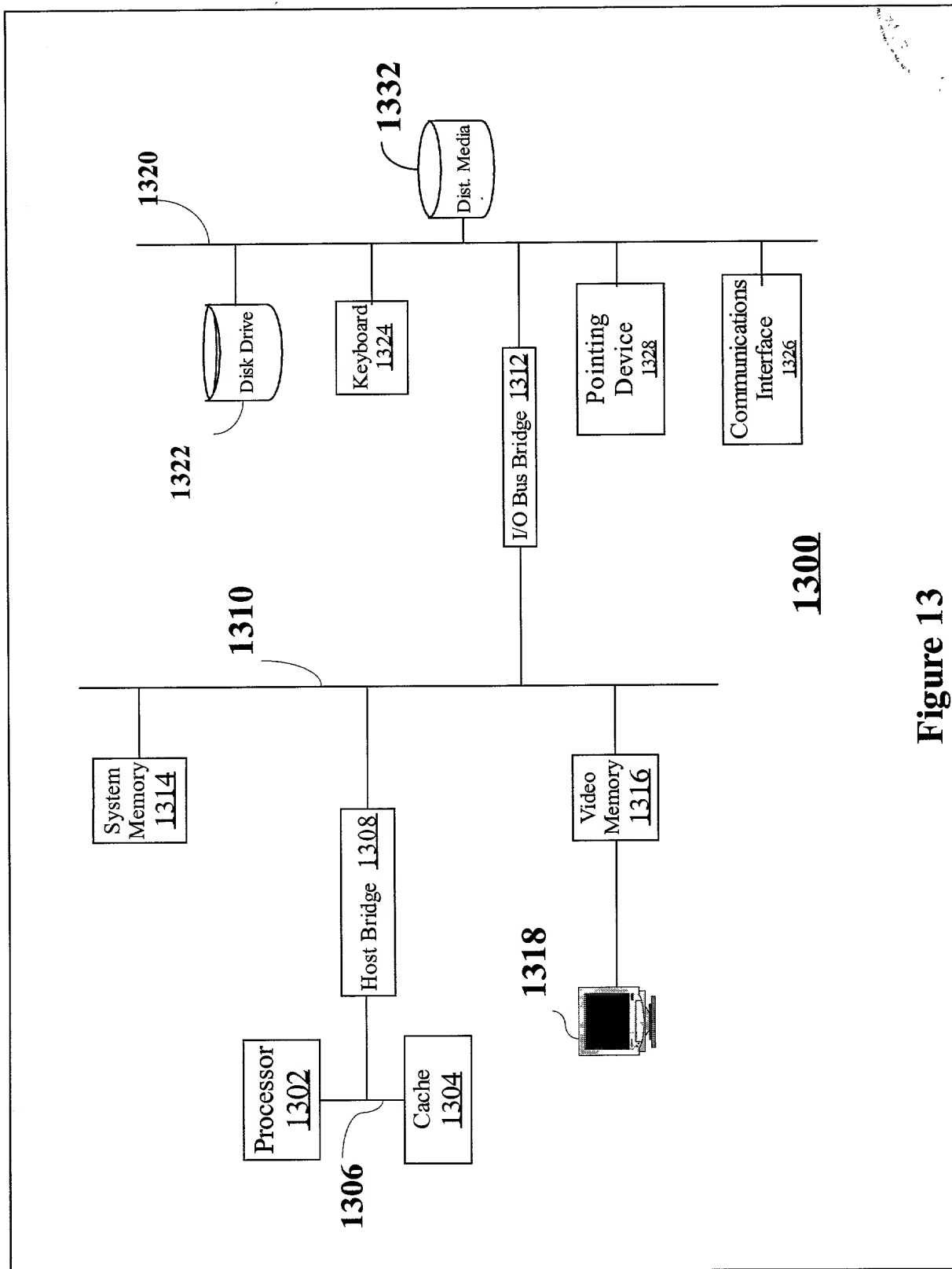


Figure 13

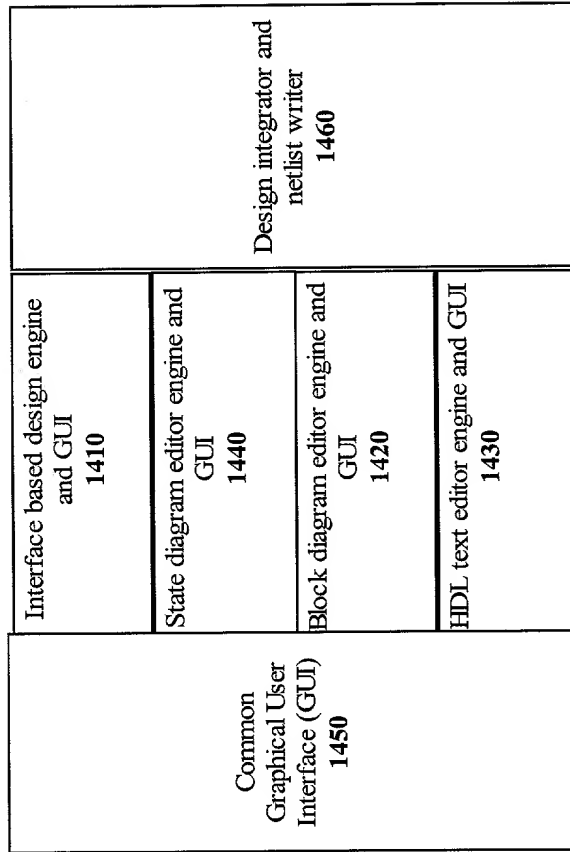


Figure 14

